A NO-PRECHARGE FAMOS CELL AND LATCH CIRCUIT IN A MEMORY DEVICE

RELATED APPLICATION

[0001] This application claims priority to Italian Patent Application Serial No. RM2003A000329, filed July 7, 2003, entitled "A NO PRE-CHARGE FAMOS CELL AND LATCH CIRCUIT IN A MEMORY DEVICE," which is commonly assigned.

TECHNICAL FIELD OF THE INVENTION

[0002] The present invention relates generally to memory devices and in particular the present invention relates to fuse cells and latches in memory devices.

BACKGROUND OF THE INVENTION

[0003] Flash memory devices have developed into a popular source of non-volatile memory for a wide range of electronic applications. Flash memory devices typically use a one-transistor memory cell that allows for high memory densities, high reliability, and low power consumption. Common uses for flash memory include portable computers, personal digital assistants (PDAs), digital cameras, and cellular telephones. Program code, system data such as a basic input/output system (BIOS), and other firmware can typically be stored in flash memory devices. Most electronic devices are designed with a single flash memory device.

[0004] Flash memory devices typically use Floating gate Avalanche injection Metal Oxide Semiconductor (FAMOS) cells, also referred to as fuses, to store device information. This information may include the address of defective memory array columns or rows and analog circuit configuration. The fuses are associated with latches in order to make the data stored in the fuse constantly available without the need for a typical flash memory read operation through the sense amplifiers.

[0005] Figure 1 illustrates a schematic diagram of a typical prior art fuse and latch. In this scheme, the READ signal for the n-channel transistor 105 is normally in a logical low

state. This turns off the transistor 105 and isolates the fuse 101. The signal FUSE_CLEAR is low to turn off the n-channel transistor 103, making it not effective. The signal PRE_CHARGE is high to turn off the p-channel transistor 113, making it not effective. The signal FSLTCH_BIAS is an analog signal that assumes a value between V_{cc} and V_{ss}. That signal is normally low to turn on p-channel transistor 111, allowing the latch made by the inverter 107 and by the transistors 109 and 110, to be properly supplied by V_{cc}. To read the fuse 101, the signals PRE_CHARGE, FSLTCH_BIAS and READ are operated in sequence in two separate time intervals. In the first time interval, usually referred to as the precharge operation, while the READ and FSLTCH_BIAS signals are still low, the signal PRE_CHARGE goes low and therefore the p-channel transistor 113 is turned on to force the node OUTB at V_{cc}. Therefore the inverter 107, having at its input V_{cc}, turns low (V_{ss}) the node OUT and this, throughout the transistors 109 and 110, confirms (latches) the node OUTB ad V_{cc}. In the second time interval, usually referred to as the sensing operation, the signal PRE_CHARGE goes back high, so that the p-channel transistor 113 is turned off, while the signal READ goes high, so that the n-channel 105 transistor is turned on to connect the fuse 101 to the latch structure. In addition, during the second time interval the signal FSLTCH_BIAS goes to an intermediate value between V_{ss} and V_{cc}, so that the p-channel transistor 111 is still turned on, while its capability to conduct current is strongly reduced. That way, the series of the two p-channel transistors 111 and 109 will not be able to contrast the current eventually driven by the fuse 101 and flowing throughout the n-channel transistor 105. If the fuse 101 is programmed, a low current will flow from V_{cc} to V_{ss} throughout the transistors 111, 109, 105 and the fuse 101 and a logical low signal is at the input of the inverter 107. Therefore, the latch transistors 109 and 110 receive a logical high output from the inverter 107 and confirm (latch) the logical low at node OUTB. If the fuse 101 is erased no current flows through it, the latch transistors 109 and 110 receive a logical low from the inverter 107 and confirm (latch) the logical high at node OUTB.

[0006] When the prior art circuit of Figure 1 must be cleared (this usually happens during testing operations only, while still in the factory), the fuse_clear signal is brought to a logical high to turn on the n-channel transistor 103, while the signal PRE_CHARGE is maintained high to turn off transistor 113. This allows current to flow from Vcc through

the p-channel transistors 111 and 109 and the n-channel transistor 103 to ground. This provides a logical high to the latch transistors 109 and 110, thus placing the latch into a default "erased" state before it receives its proper value from the fuse 101.

[0007] When a reset operation of the device occurs, both at power up and when the user applies to the device the proper reset pulse, this usually requires that, the latch must be reloaded with the proper ("erased" or "programmed") data from the fuse 101. This managed, as explained above, in two distinct time intervals, is commonly referred to as the precharge and the sensing operations. The precharge operation reduces the speed at which the memory can respond after a reset condition has been experienced. An additional problem is that if a reset pulse is stopped too early for some reason, the proper value may not be reloaded into the latch and this error condition may not be detectable before causing additional errors to occur from the corrupted latch data.

[0008] For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a fuse and latch circuit that does not require a precharge operation.

SUMMARY

[0009] The above-mentioned problems with precharging a fuse and latch circuit and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

[0010] The various embodiments relate to a fuse and latch circuit that can be read after an initialization or reset operation that occurs during the power up only, without precharging from the fuse. The circuit includes a fuse that has either a programmed state or an erased state. The fuse, in one embodiment, is a Floating gate Avalanche injection Metal Oxide Semiconductor (FAMOS) cell. A latch that stores either the programmed state or the erased state from the fuse is coupled to the fuse through a transfer circuit. A fuse read circuit is coupled to the fuse and a READ signal, in order to sense the state of the fuse.

[0011] The transmission circuit, in one embodiment, is a transfer gate. This circuit isolates the latch in response to the PRE_CHARGE signal such that the state stored in the latch remains after the read signal indicates completion of a read operation.

[0012] Further embodiments of the invention include methods and apparatus of varying scope.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Figure 1 shows a schematic diagram of a typical prior art precharge fuse.

[0014] Figure 2 shows a block diagram of one embodiment of the no-precharge FAMOS cell and latch circuit of the present invention.

[0015] Figure 3 shows a block diagram of one embodiment of a driver circuit of the present invention.

[0016] Figure 4 shows a schematic diagram of one embodiment of the no-precharge FAMOS cell and latch circuit in accordance with the embodiment of Figure 2.

[0017] Figure 5 shows a schematic diagram of an alternate embodiment of the no-precharge FAMOS cell and latch circuit in accordance with the embodiment of Figure 2.

[0018] Figure 6 shows a block diagram of one embodiment of a memory system that incorporates the no-precharge FAMOS cell and latch circuit of the present invention.

DETAILED DESCRIPTION

[0019] In the following detailed description of the invention, reference is made to the accompanying drawings that form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present

invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims and equivalents thereof.

[0020] Figure 2 illustrates a block diagram of one embodiment of the no-precharge FAMOS cell and latch circuit of the present invention. The circuit has a flash FAMOS transistor cell 201 that is subsequently referred to as a fuse. The fuse 201 has two states: erased and programmed. In the erased state, the FAMOS transistor that makes up the fuse 201 is able to conduct current to ground. In the programmed state, the transistor cannot conduct current. A signal that for most applications reaches the voltage of about 4.5V, is placed on a WORDLINE in order to read the data from the fuse 201. The read operation of the fuse 201 is well known in the art and is not discussed further.

[0021] A FAMOS read circuit 203 is coupled to the fuse 201 to either isolate the fuse 201 or allow the fuse data to be read out, depending on the state of the input signals FSLATCH_BIAS and READ. One embodiment for generating these signals is described subsequently with reference to the driver circuit of Figure 3.

[0022] The FSLATCH_BIAS signal, in one embodiment, is an analog signal normally at an intermediate value between V_{cc} and ground such signal that it reduces the current of the read circuit 203 to allow the proper sensing of the fuse 201. The READ signal is a normally low signal that isolates the fuse 201 from the rest of the circuit. When READ is high, the read circuit 203 is enabled and the fuse state can be read.

[0023] A FUSE_CLEAR signal clears the latch 211 to a default state. In one embodiment, the default state is a logical high. When the FUSE_CLEAR signal goes to a logical high state, a clear circuit 209 sets the latch to the logical high state. This is the erased state of the fuse 201. An alternate embodiment uses a logical low state as the default state and/or a logical low state for the FUSE_CLEAR signal.

[0024] In operation, the circuit 200 is initialized by a power-on reset and the fuse latch is initially assumed to be cleared (i.e., in the state corresponding to an erased fuse). This is not mandatory for the proper functioning of the invention, that works correctly also with the latch initially in the opposite state. Anyway, the initial clearing of the latch can be

obtained in several manners, e.g. by dividing the power up RESB signal into two parts and by using its first part to generate the FUSE_CLEAR signal. As discussed subsequently with reference to Figure 3, the READ signal is high while FSLTCH_BIAS signal is at an intermediate value between V_{cc} and ground and FSLATCH_BIAS signals during a power-on reset operation. If the fuse is erased (i.e. the FAMOS cell is conducting), This causes the FAMOS read circuit 203 to generate a logical low signal at FUSE_READ_b and, therefore, a logical high signal at the output of the inverter 205. The FUSE_CLEAR signal is supposed to be low during this operation.

[0025] The READ signal and its inverse, READ_b, enable a transmission gate 207 to allow the logical signal from the inverter 205 to be input to the latch 211. This signal is now the OUT signal as well. The transmission gate 207 or other type of transfer/isolation circuit isolates the latch from the rest of the circuit when it is not enabled. Alternate embodiments may use other types of transfer/isolation circuits than the transmission gate of the present invention. For example, a high impedance buffer circuit may perform a substantially similar function.

[0026] After the fuse is programmed (i.e., non-conducting) a read operation may be executed by bringing WORDLINE high. If READ is also a logical high, this causes the output of the FAMOS read circuit 203 to be a logical high (i.e., FUSE_READ_b = high). Therefore, the output of the inverter 205, FUSE_READ, is a logical low signal. Since READ and READ_b are active, the transmission gate 207 is turned on and the logical low signal is set in the latch 211 and is now the OUT signal.

[0027] Both in the cases the FAMOS cell is erased or programmed, the content of the FAMOS cell is directly transferred into the latch while the signal READ is high, i.e. during the reset operation (signals RESB or RP# low). Therefore, unlike the prior art fuse, the present invention provides the fuse 201 contents already in the latch 211 as soon as the reset operation has been completed. There is no need to precharge the fuse latch circuit 200, thus enabling a memory circuit incorporating the fuse latch circuit to respond faster to latch read operations. One implementation of this block diagram is illustrated subsequently with reference to Figure 4.

[0028] Figure 3 illustrates one embodiment for a driver circuit of the present invention. This figure is for purposes of illustration only and does not limit the present invention to any one circuit for generating the signals required for proper operation of the no-precharge FAMOS cell and latch circuit.

[0029] A NAND gate 301 has one input tied to a power-on reset signal "RESb". The RESb signal is low when a power-on reset condition is experienced.

[0030] A CAMRES_PULSE_GENERATOR circuit 305 generates a signal indicating a user reset condition. This may occur due to a user initiating a reset as opposed to a power-on reset condition. The CAMRES_PULSE_GENERATOR circuit 305, in one embodiment, generates a low-going pulse that is low for a predetermined time. The generator 305 may be a one-shot circuit that generates a low pulse (CAMRES_PULSE), having a width of approximately 30 ns, on the falling edge of the user reset. However, alternate embodiments use other generators, states, and pulse widths to indicate the user reset condition.

[0031] The CAMRES_PULSE is input to the NAND gate 301. The NAND gate 301 then outputs a logical high pulse signal (READ) whenever either a power-on reset condition or a user reset condition is experienced. READ, therefore, is an active high reset indication signal. Alternate embodiments use other states and/or types of logic to indicate a power-on or user reset condition.

[0032] An inverter 307 has its input tied to READ signal and outputs the logical signal READ_b. READ_b always has the opposite logical value of the signal READ and is provided to the NO-PRECHARGE FAMOS CELL AND LATCH CKT circuit 200.

[0033] A FSLATCH_BIAS_GENERATOR 303 is connected to the output of the NAND gate 301. A high pulse READ signal causes the FSLATCH_BIAS_GENERATOR 303 to generate the FSLATCH_BIAS signal to the fuse latch circuit 200 of the present invention. The FSLATCH_BIAS signal is a voltage that, once applied to the FAMOS read circuit 203 of Figure 2, reduces the current of a read circuit transistor to an appropriate value to allow the proper sensing of the FAMOS cell 201. In one embodiment, the FSLATCH_BIAS signal has an intermediate value between V_{cc} and ground, that make the

read circuit transistor driving the maximum current when at ground, while switching off that transistor when at V_{cc}. Methods for generating the FSLATCH_BIAS signal from the READ signal are well known in the art and are not discussed further.

[0034] The FUSE_CLEAR signal, in one embodiment, is coupled to a power-up reset signal or test reset signal. When coupled to a power-up reset signal, it must be avoided that FUSE_CLEAR and READ signals go at a logical high contemporarily, and, in addition, the FUSE_CLEAR signal must precede the READ one. This can be easily obtained with standard design techniques. When this signal goes high during a reset operation, the fuse latch is cleared to a default value. An alternate embodiment uses other logic levels or methods of generating this signal.

[0035] For purposes of clarity, the block diagram of Figure 3 shows only one no-precharge FAMOS cell and latch circuit 200. However, a typical memory device may be comprised of thousands of these circuits.

[0036] Figure 4 illustrates a schematic diagram of one implementation of the block diagram of the no-precharge FAMOS cell and latch circuit 200 of Figure 2. The present invention is not limited to any one circuit architecture in generating the same or similar results as the fuse latch circuit 200 such that the latch retains the fuse contents even after a reset operation.

[0037] The circuit 200 includes the FAMOS cell 201 that includes the WORDLINE read input. The fuse 201 and its relevant operational characteristics were discussed previously.

[0038] The latch circuit 400 is comprised of four transistors 412 – 415. Two of the transistors are n-channel transistors 414 and 415. The other two transistors are p-channel transistors 412 and 413. Alternate embodiments may use a different architecture to form the latch circuit 400.

[0039] An n-channel transistor 405 is used as a reset circuit in conjunction with the FUSE_CLEAR signal. When this signal is a logical high, the transistor 405 is turned on

and conducts such that OUT_b is a logical low and, therefore, OUT is a logical high. The latch circuit 400 is thus reset to a default logical high state.

[0040] In the embodiment illustrated in Figure 4, a p-channel transistor 407 pulls up the FUSE_READ_b node. It is possible to make it easier to read the fuse cell 201 by reducing the transistor 407 drive strength, applying to its gate the proper FSLTCH_BIAS voltage. Similar results can be achieved in alternate embodiments by connecting the gate of the transistor 407 to V_{ss} and enlarging the channel width of the cell. Still other embodiments can achieve substantially similar results with different methods and/or circuit components.

[0041] Assuming that the fuse 201 is erased (i.e., conducting), when WORDLINE is a logical high for a read operation and READ is a logical high, the transistor 403 coupled to the READ line is turned on. The FSLATCH_BIAS signal is normally at an intermediate voltage between V_{cc} and V_{ss}, so that the p-channel transistor 407 maintains a current flowing through it lower than one that the fuse 201 is capable of supplying. FUSE_LATCH_b, therefore, is driven to a voltage below the inverter 409 threshold. The inverter 409 produces a logical high signal, FUSE_READ as an input to a transmission gate 411.

[0042] The signal READ being high and, thus, READ_b being low turns on the transmission gate 411. The logical high FUSE_READ signal is output to the latch circuit 400. Thus, OUT is kept at a logical high level.

[0043] Assuming that the fuse 201 is programmed (i.e., non-conducting), when an attempt is made to read the fuse 201 the p-channel transistor 407 pulls up the FUSE_READ_b node to a logical high state. FUSE_READ is therefore a logical low signal. When the transmission gate 411 is turned on by the READ and READ_b signals, the logical low signal is output to the latch circuit 400. OUT is now a logical low signal.

[0044] After the power-up, if the memory device is reset by the user (i.e., by RP# external signal), READ goes to a logical high state and turns on the n-channel transistor 403. Since the fuse 201 was programmed and does not drive current, the FUSE_READ_b node is still pulled up to a logical high state. Therefore, the OUT signal does not change

after a reset operation. The value stored in the fuse latch circuit 200 is available for immediate use without waiting to be reloaded into the latch as required by the prior art.

[0045] Figure 5 illustrates an alternate circuit architecture of the block diagram of the fuse latch circuit 200 of Figure 2. This embodiment accomplishes the same results as the embodiment of Figure 4 but uses a greater number of transistors.

[0046] This embodiment is comprised of the same FAMOS cell (fuse) 201 and latch circuit 400 as used in Figure 4. Additionally, the FUSE_CLEAR transistor 405, n-channel READ transistor 403, and p-channel current limiting transistor 407 are similarly used.

[0047] A p-channel transistor 501 is used to put the latch 400 into the "programmed" state while an n-channel transistor 502 puts the latch 400 into the "erased" state. These transistors 501 and 502 are controlled by a logic control circuit comprising logic gates 503 – 505 in order to put the latch 400 into the proper state.

[0048] In one embodiment, the logic control circuit includes a NAND gate 503 with one input coupled to the FUSE_READ_b node and the other input coupled to the READ signal. An inverter 504 has an input coupled to the READ signal and generates the READ_b signal. A NOR gate 505 has one input coupled to the FUSE_READ_b node and another input coupled to the READ_b signal. Alternate embodiments use other logic gate configurations to achieve substantially the same results.

[0049] If the fuse is erased, FUSE_READ_b is at a logical low level. Therefore, READ_b is a logic high and signal READ_bb is also high. In this case, the n-channel "erased" transistor 502 is turned on and the p-channel "programmed" transistor 501 is turned off. The latch 400 is loaded with a logic high state. The signal OUT, therefore, is now a high.

[0050] If the fuse is programmed, FUSE_READ_b is at a logic high level. Therefore, READ_b is a logic low and READ_bb is also a low. In this case, the p-channel "programmed" transistor 501 is turned on and the n-channel "erased" transistor is turned off. The latch is loaded with a logic low state. The signal OUT, therefore, is now a low.

[0051] Figure 6 illustrates a functional block diagram of a memory device 600 of one embodiment of the present invention that is coupled to a processor 610. The processor 610 may be a microprocessor, a processor, or some other type of controlling circuitry. The memory device 600 and the controller 610 form part of an electronic system 620. The memory device 600 has been simplified to focus on features of the memory that are helpful in understanding the present invention.

[0052] The memory device 600 includes an array of memory cells 630. The memory cells are non-volatile floating-gate memory cells and the memory array 630 is arranged in banks of rows and columns. In one embodiment, the memory array is a NAND-type architecture. In another embodiment, the memory array is a NOR-type architecture. The present invention is not limited to any one type of memory array architecture. The no-precharge FAMOS cell and latch circuit of the present invention may be located in the memory array 630 or any other location in the device 600.

[0053] An address buffer circuit 640 is provided to latch address signals provided on address input connections A0-Ax 642. Address signals are received and decoded by a row decoder 644 and a column decoder 646 to access the memory array 630. It will be appreciated by those skilled in the art, with the benefit of the present description, that the number of address input connections depends on the density and architecture of the memory array 630. That is, the number of addresses increases with both increased memory cell counts and increased bank and block counts.

[0054] The memory device 600 reads data in the memory array 630 by sensing voltage or current changes in the memory array columns using sense/latch circuitry 650. The sense/latch circuitry, in one embodiment, is coupled to read and latch a row of data from the memory array 630. Data input and output buffer circuitry 660 is included for bi-directional data communication over a plurality of data connections 662 with the controller 610). Write/erase circuitry 655 is provided to write data to the memory array.

[0055] Control circuitry 670 decodes signals provided on control connections 672 from the processor 610. These signals are used to control the operations on the memory array 630, including data read, data write, and erase operations. In one embodiment, the control

circuitry 670 is a microcontroller that executes the embodiments of the automatic test entry termination methods of the present invention.

[0056] Chip select generation circuitry 625 generates the chip select signals for the memory device 600. This circuitry 625 uses the address connections 642 from the processor 610 to generate the appropriate chip select signal depending on the address present on the address connections 642.

[0057] The fuses/latches array 685 comprises the no-precharge FAMOS cell and latch circuit of the present invention. In this embodiment, the circuit interacts with the control registers 680, the write/erase circuit 655, the row decode644, and the column decode 646.

[0058] The flash memory device illustrated in Figure 6 has been simplified to facilitate a basic understanding of the features of the memory. A more detailed understanding of internal circuitry and functions of flash memories are known to those skilled in the art.

CONCLUSION

[0059] In summary, the no-precharge FAMOS cell and latch circuit of the present invention enables a memory device to be read immediately after a reset operation without waiting to precharge the latch with data from the cell. This is accomplished by providing a fuse and latch architecture that maintains the data after the reset operation.

[0060] Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiments shown. Many adaptations of the invention will be apparent to those of ordinary skill in the art. Accordingly, this application is intended to cover any adaptations or variations of the invention. It is manifestly intended that this invention be limited only by the following claims and equivalents thereof.